AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Original) An integrated circuit device having a semiconductor substrate, comprising:

a memory cell array comprising a plurality of volatile memory cells; and

a metal oxide semiconductor field effect transistor (MOSFET) configured as a non-volatile electrically erasable programmable read only memory (EEPROM) device having a floating gate and a control gate, and adapted to store status information associated with the memory cell array,

wherein the MOSFET has a single polysilicon film for the floating gate, and the control gate is disposed within a well in the semiconductor substrate.

2. (Original) The device as claimed in 1, wherein the control gate of the MOSFET corresponds to a second conductive ion-implantation region which is spaced from a channel region of the MOSFET and which is formed under the single polysilicon film.

3. (Original) The device as claimed in 2, wherein the MOSFET is an n-channel MOSFET, and a program operation for electrically programming the EEPROM is performed by injecting electrons into the floating gate through a hot electron injection method.

4. (Original) The device as claimed in 3, wherein an erase operation for the EEPROM is performed by discharging the electrons captured by the floating gate through an F-N (Fowler-Nordheim) tunneling process.

5-15. (Canceled)